SEMICODUCTOR PASSIVATION USING BARRIER COATINGS

This application is a continuation-in-part of U.S. patent application Ser. No. 09/427138, filed Oct. 25, 1999, entitled "Environmental Barrier Material For Organic Light Emitting Device And Method Of Making."

BACKGROUND OF THE INVENTION

The present invention relates generally to microelectronic devices, and more particularly to microelectronic devices encapsulated in barrier stacks.

Microelectronic devices fabricated on semiconductor substrates require passivation, or encapsulation, to protect them from atmospheric contaminants and constituents, mechanical damage, stress, thermal stress and cycling, downstream processing, and corrosive chemicals.

Passivation of the microelectronic devices performs several functions. First, it electrically insulates the microelectronic device from other microelectronic devices. It preserves the recombination velocity at the semiconductor surface. It is also a stress buffer to minimize cracking. It provides protection from processing chemicals, ultraviolet light exposure, and photoresists during lithography processes. In addition, it provides protection from humidity, oxidants, corrosive materials, scratching, and mechanical damage. Finally, it provides gettering of mobile ions, such as Cl^-, and Na^+. Lavinger et al., J. Vac. Sci. Technol. A16(2), Mar./Apr. 1998, p.530.

Conventional hermetic sealing in metal or ceramic provides effective protection. However, conventional hermetic enclosures are relatively bulky (about 4–6 mm deep), and they add a significant amount of weight to the product, which reduces the benefits of miniaturization.

Many devices that require passivation are now fabricated on glass, fused silica, and ceramic substrates. For example, thin films of amorphous silicon nitride (Si_3N_4) and silicon dioxide (SiO_2) are used on p-type semiconductor devices as a protective coating, a mask for lithography processes, charge storage systems in nonvolatile metal-nitride-oxide-semiconductor memory devices, insulators between metal layers, gate insulators for thin film transistors, and ultrathin dielectrics for very large scale integration devices. For integrated circuit applications, SiO_2 is the stress buffer layer and Si_3N_4 is the passivation layer, as described in U.S. Pat. No. 5,851,603, which is incorporated herein by reference. Silicon nitride is primarily deposited by chemical vapor deposition processes (CVD), such as atmospheric pressure chemical vapor deposition (APCVD), low pressure chemical vapor deposition (LPCVD), and plasma enhanced chemical vapor deposition (PECVD). However, the use of inorganic materials deposited by standard semiconductor processes such as chemical vapor deposition has several disadvantages. The most serious disadvantages are brittleness, a tendency to crack under mechanical stress, poor step coverage, poor planarization properties, and poor barrier properties. The best oxygen permeation rate for Si_3N_4 deposited by electron cyclotron resonance-plasma enhanced vapor deposition (ECR PECVD) is reported to be near 1 $cc/m^2/day$. The best oxygen permeation rate for SiO_2 is also near 1 $cc/m^2/day$.

As a result of these problems, there has been a significant effort to replace inorganic materials such as SiO_2 and Si_3N_4 with polymer dielectrics. Polymer materials of interest include polyimide, polyamide, and paralyene. Organic materials offer good adhesion, sufficient elasticity, and sufficient tensile strength. However, these materials have problems with brittleness and defects such as voids. C. P. Wong, Ceramic Trans. 33, 1993 p. 125.

The barrier protection offered by inorganic and organic materials is not usually adequate to ensure reliable microelectronic device operation. Additional barrier layers are added prior to encapsulation. Materials such as silicon rubber are used as barriers. The integrated circuit can be embedded in plastic by injection molding to add further moisture barrier protection.

Epoxies are also used for barrier applications and encapsulation. The epoxy layers used for encapsulation are only about one quarter of the thickness of the layers required for convention hermetic sealing. However, even that thickness produces a device which is unacceptably heavy and bulky in many applications. In addition, epoxies have a water vapor permeation rate which is too high for some applications.

The passivation layers currently being used in microelectronics include silicon dioxide, silicon nitride, and silicon oxynitride layers with thicknesses up to about 1 μm. These layers are deposited by CVD and reactive magnetron sputtering processes, which can require substrate and processing temperatures as high as 800° C. Materials deposited by CVD can also have very stresses (i.e., greater than 10,000 MPa).

The inorganic layer is often followed by a spin cast polyimide layer about 0.5 μm thick. The polyimide layer is used for passivation, encapsulation, planarization, and bonding/molding to the packaging. The layer is spun on and cured at temperatures up to 250° C. The oxygen and water vapor barrier properties of polyimide are poor and typical of polymer substrates (>10 $cc/m^2/day$). Polyimide is very opaque and strongly absorbing at visible wavelengths. Polyimide films can have large numbers of voids, which can cause reliability problems with integrated circuits. The voids can also cause hot spots and cracks that can damage integrated circuit components.

Another method used to protect microelectronic circuitry is vapor deposition of a thin film of parylene. However, the water vapor permeation rate of the parylene is too high for many applications. In addition, parylene is subject to thermal oxidation at temperatures over about 120° C.

Furthermore, PECVD coatings have problems with pinholes, poor step coverage, and particulates. The quality of the coating is usually poor. Deposition processes for these layers can damage temperature sensitive material in, for example, integrated circuits, organic light emitting devices, light emitting polymers and microlasers. As a result, totally effective encapsulation of temperature sensitive devices cannot be achieved on semiconductor substrates using conventional deposition processes. Additionally, in order to obtain the required encapsulation and passivation, the current passivation layers must be thick compared to device thicknesses and sizes, which causes problems in the fabrication of multilevel integrated circuits. Finally, as discussed above, the barrier properties for these materials are inadequate for many applications.

Thus, there is a need for an improved, lightweight, thin film, barrier construction which can be used to encapsulate microelectronic devices, and for methods for making such encapsulated microelectronic devices.

SUMMARY OF THE INVENTION

The present invention meets these needs by providing an encapsulated microelectronic device and a method for making such a device. The device includes a semiconductor substrate, a microelectronic device adjacent to the semicon-